参考資料

COSEL

TUNS700F series Safety test result

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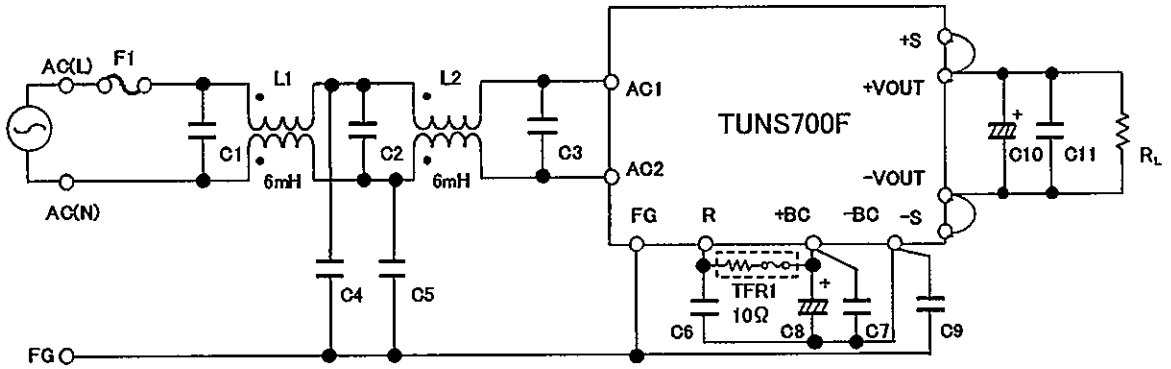
OS DESIGN DEPT.

Approved: Takayuki Fukuda
Takayuki Fukuda

Prepared: Ryosuke Nakao
Ryosuke Nakao

No.	Test item	Test conditions	Conditions of acceptability	Result
1	High temp./overload test	(1) Input Rated input (AC100V,200V) (2) Output Overload (3) Baseplate temp. 50°C (Output voltage 12) 70°C (Output voltage 28,48) (4) Test period 48 hours (5) Testing circuitry Fig.1	(1) Power supply is not failed.	ok
2	Capacitance reduction test	(1) Input Rated input (AC100V) (2) Output Rated output (3) Ambient temp. 25±10°C (4) Testing circuitry Fig.1	(1) No smoke, no fire. (2) No rise of the output voltage.	ok
3	Low voltage input test	(1) Input Min. regulation voltage (2) Output Rated output (3) Ambient temp. 25±10°C (4) Test period 48 hours (5) Testing circuitry Fig.1	(1) Power supply is not failed.	ok
4	Input ON/OFF test	(1) Input Rated input (AC200V) T= 2sec Duty= 50% (2) Output Rated output (3) Ambient temp. 25±10°C (4) On/off period 1,000 (5) Testing circuitry Fig.1	(1)Power supply is not failed. (2)The surge current of each components should not exceed the rated value.	ok
5	Output ON/OFF test	(1) Input Rated input (AC100V) (2) Output 0%←→100% T= 2sec Duty= 50% (3) Ambient temp. 25±10°C (4) On/off period 1,000 (5) Testing circuitry Fig.1	(1) Power supply is not failed.	ok
6	Output-short start test	(1) Input Max. voltage (AC264V) (2) Output Short start (3) Ambient temp. 25±10°C (4) Testing circuitry Fig.1	(1) Power supply is not failed.	ok
7	Output short test	(1) Input Rated input (AC100V,200V) (2) Output Short (3) Ambient temp. 25±10°C (4) Test period 48 hours (5) Testing circuitry Fig.1	(1) Power supply is not failed.	ok
8	Withstand voltage test (High-pot test)	(1) Input Not applied. (2) Ambient temp. 25±10°C (3) The applied voltage is 1.4 times of specifications.	(1) Insulation breakdown ,flashover or electric arc is not occurred.	ok
9	Isolation resistance test	(1) Input Not applied. (2) Ambient temp. 25±10°C	(1) When a regulation voltage is applied, isolation resistance is 1.4 times of specifications.	ok
10	Vibration/impact test	Vibration (1)f=10～55Hz : 49.0m/s² (2)3 minutes period (3)60 minutes along X, Y and Z axis Impact (1)196.1m/s² 11ms (2)Once each X, Y and Z axis	(1) No degradiation of electric characteristics after test. (2) No crack at solder joint. (3) No marked damage of appearance.	ok
11	Line Noise Tolerance test	(1) Input AC230V (2) Output Rated output (3) Ambient temp. 25±10°C (4) Test Voltage ±2 kV (5) Pulse width 50～1000ns (6) Mode Normal and Common (7) Testing circuitry Fig.1	(1) No protection circuit failure. (2) No output voltage drop with control circuit failure. (3) No any other function failure.	ok

○ Testing circuitry



L1,L2 : ADM-25-12-060T(Ueno)
C1,C2 : 1.5μF 275V Film Capacitor
C3 : 1.5μF 275V Film Capacitor × 2
C4,C5,C9 : 2200pF Ceramic Capacitor
C6,C7 : 0.68μF 450V Film Capacitor × 2
C8 : 390μF 450V Electrolytic Capacitor × 2
C10 : TUNS700F12 2200μF 25V Electrolytic Capacitor
TUNS700F28 1000μF 50V Electrolytic Capacitor
TUNS700F48 470μF 63V Electrolytic Capacitor

C11 : TUNS700F12 10μF Ceramic Capacitor
TUNS700F28 4.7μF Ceramic Capacitor
TUNS700F48 2.2μF Ceramic Capacitor

Fig.1 Testing circuitry